Amendments to the claims:

Please Cancel Claims 1 and 4.

Please Amend Claims 2 and 3 as follows:

2. (Once Amended)[A sigma delta quantizer circuit according to Claim 1,]
A sigma delta circuit comprising:

a sigma delta modulator configured to operate according to a first clock signal; and

a quantizer connected to the sigma delta modulator and configured to operate according to a second clock signal, wherein the sigma delta modulator is further configured to operate at a fixed output frequency of transitions under one set of circumstances, and to operate at a variable frequency under another set of circumstances.

3.[4]. (Once Amended)[A sigma delta circuit according to Claim 1]
A sigma delta circuit comprising:

a sigma delta modulator configured to operate according to a first clock signal; and

a quantizer connected to the sigma delta modulator and configured to operate according to a second clock signal, wherein the sigma delta quantizer element is configured to operate at a variable clock frequency such that for small input signals a fixed frequency of output transition is produced and for large input signals a possibly variable output frequency of edges is produced

5. A sigma delta circuit according to Claim 1, wherein the second clock signal that determines the output frequency of transitions is a variable clock signal.

PAGE 2/3 * RCVD AT 8/11/2004 4:04:36 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/5 * DNIS:8729306 * CSID:408 288 7542 * DURATION (mm-ss):01-08